

FIG. 1

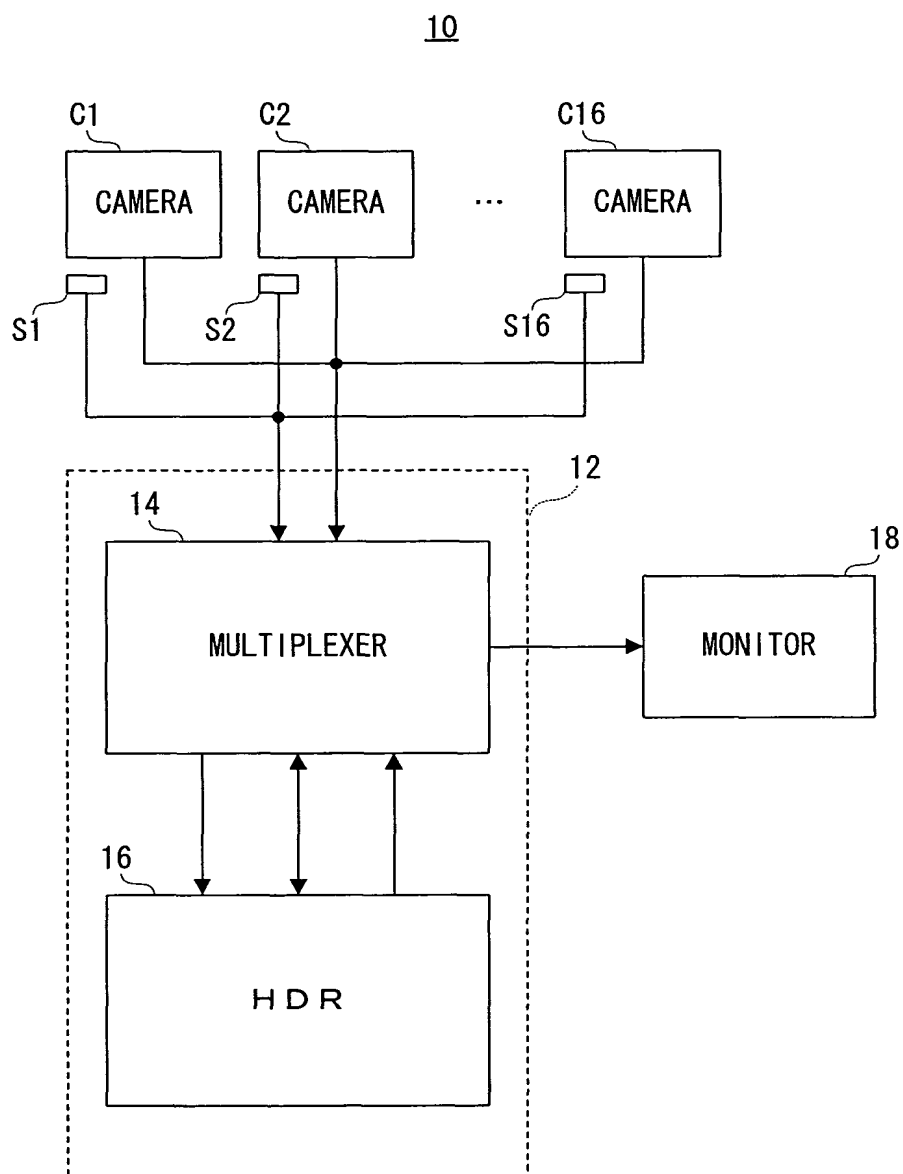


FIG. 2

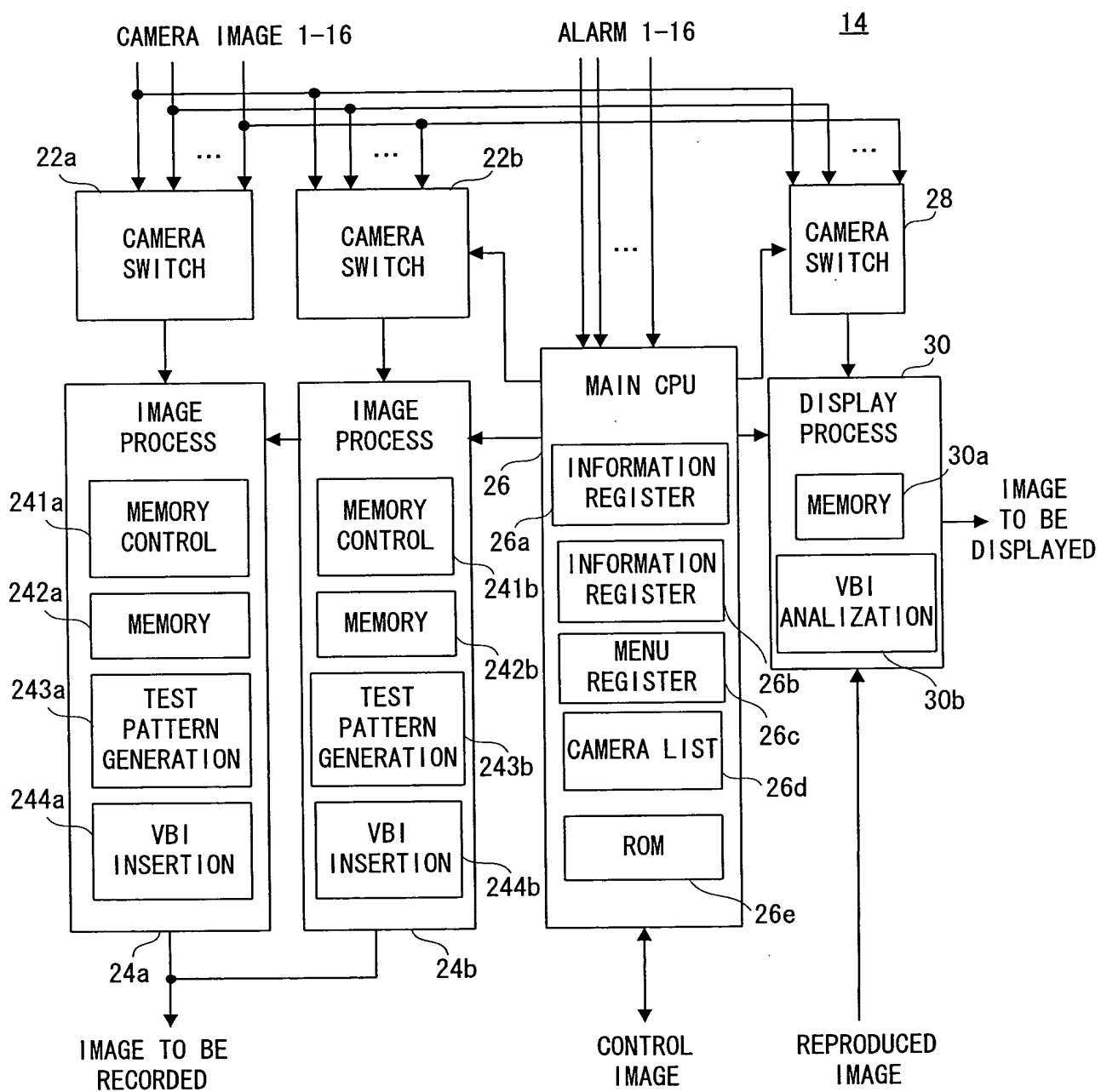


FIG. 3

	FIELD	1	2	3	4	1
CAMERA SWITCH CIRCUIT 22a	OPERATION	CAMERA SWITCH				CAMERA SWITCH
IMAGE PROCESS CIRCUIT 24a	OPERATION	OUTPUT CAMERA IMAGE OR PATTERN IMAGE	STORE CAMERA IMAGE	STORE CAMERA IMAGE	OUTPUT PATTERN IMAGE	OUTPUT CAMERA IMAGE OR PATTERN IMAGE
	FIELD	3	4	1	2	3
CAMERA SWITCH CIRCUIT 22b	OPERATION			CAMERA SWITCH		
IMAGE PROCESS CIRCUIT 24b	OPERATION	STORE CAMERA IMAGE	OUTPUT PATTERN IMAGE	OUTPUT CAMERA IMAGE OR PATTERN IMAGE	STORE CAMERA IMAGE	STORE CAMERA IMAGE
FINAL OUTPUT		CAMERA IMAGE OR PATTERN IMAGE	PATTERN IMAGE	CAMERA IMAGE OR PATTERN IMAGE	PATTERN IMAGE	CAMERA IMAGE OR PATTERN IMAGE

FIG. 4

<RECORDING MODE SETTING>	
NORMAL RECORDING MODE	: ON ; P-1
PRE-ALARM RECORDING MODE	: OFF
POST-ALARM RECORDING MODE	: 30FPS

FIG. 5

<PROGRAM RECORDING SETTING>			
P-1			
01:15.0	02:7.5	03:OFF	04:OFF
05:OFF	06:OFF	07:OFF	08:OFF
09:OFF	10:OFF	11:OFF	12:OFF
13:OFF	14:OFF	15:OFF	16:OFF

FIG. 6

CAMERA SWITCH 22a, IMAGE PROCESSING 24a	FIELD	1	2	3	4	1	2	3	4	1	2	3	4
	SELECTED CAMERA	1	1	1	1	1	1	1	1	1	1	1	1
	OUTPUT CANDIDATE	1/T			T	1/T			T	1/T			T
CAMERA SWITCH 22b, IMAGE PROCESSING 24b	FIELD	3	4	1	2	3	4	1	2	3	4	1	2
	SELECTED CAMERA	2	2	2	2	2	2	2	2	2	2	2	2
	OUTPUT CANDIDATE		T	2/T			T	2/T			T	2/T	
FINAL OUTPUT		1	T	2	T	1	T	T	T	1	T	2	T
VBI	RECORDING	1	0	1	0	1	0	0	0	1	0	1	0
	PRE-ALARM	0	*	0	*	0	*	*	*	0	*	0	*
	POST-ALARM	0	*	0	*	0	*	*	*	0	*	0	*
	ID	1	*	2	*	1	*	*	*	1	*	2	*

1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1/T			T	1/T			T	1/T			T	1/T			T
3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	T	2/T			T	2/T			T	2/T			T	2/T	
1	T	T	T	1	T	2	T	1	T	T	T	1	T	2	T
1	0	0	0	1	0	1	0	1	0	0	0	1	0	1	0
0	*	*	*	0	*	0	*	0	*	*	*	0	*	0	*
0	*	*	*	0	*	0	*	0	*	*	*	0	*	0	*
1	*	*	*	1	*	2	*	1	*	*	*	1	*	2	*

T: TEST PATTERN IMAGE

FIG. 7

<RECORDING MODE SETTING>	
NORMAL RECORDING MODE	: ON ; P-1
PRE-ALARM RECORDING MODE	: ON ; P-2
POST-ALARM RECORDING MODE	: 30FPS

FIG. 8

<PROGRAM RECORDING SETTING>			
P-2			
01:7.5	02:3.75	03:OFF	04:OFF
05:OFF	06:OFF	07:OFF	08:OFF
09:OFF	10:OFF	11:OFF	12:OFF
13:OFF	14:OFF	15:OFF	16:OFF

FIG. 9

<PROGRAM RECORDING SETTING>			
P-3			
01:OFF	02:OFF	03:7.5	04:2.5
05:OFF	06:OFF	07:OFF	08:OFF
09:OFF	10:OFF	11:OFF	12:OFF
13:OFF	14:OFF	15:OFF	16:OFF

FIG. 10

CAMERA SWITCH 22a, IMAGE PROCESSING 24a	FIELD	1	2	3	4	1	2	3	4	1	2	3	4
	SELECTED CAMERA	1	1	1	1	2	2	2	2	1	1	1	1
	OUTPUT CANDIDATE	2/T				T	1/T			T	2/T		T
CAMERA SWITCH 22b, IMAGE PROCESSING 24b	FIELD	3	4	1	2	3	4	1	2	3	4	1	2
	SELECTED CAMERA	4	4	3	3	3	3	4	4	4	4	3	3
	OUTPUT CANDIDATE		T	4/T				T	3/T			T	4/T
FINAL OUTPUT		2	T	4	T	1	T	3	T	T	T	T	T
VBI	RECORDING	1	0	1	0	1	0	1	0	0	0	0	0
	PRE-ALARM	0	*	1	*	0	*	1	*	*	*	*	*
	POST-ALARM	0	*	0	*	0	*	0	*	*	*	*	*
	ID	2	*	4	*	1	*	3	*	*	*	*	*

1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
2	2	2	2	1	1	1	1	2	2	2	2	1	1	1	1
1/T				T	2/T			T	1/T			T	2/T		T
3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2
3	3	4	4	4	4	3	3	3	3	4	4	4	4	3	3
				T	3/T			T	4/T			T	3/T		T
1	T	3	T	2	T	T	T	1	T	3	T	T	T	4	T
1	0	1	0	1	0	0	0	1	0	1	0	0	0	1	0
0	*	1	*	0	*	*	*	0	*	1	*	*	*	1	*
0	*	0	*	0	*	*	*	0	*	0	*	*	*	0	*
1	*	3	*	2	*	*	*	1	*	3	*	*	*	4	*

T: TEST PATTERN IMAGE

FIG. 11

CAMERA SWITCH 22a, IMAGE PROCESSING 24a	FIELD	1	2	3	4	1	2	3	4	1	2	3	4
	SELECTED CAMERA	5	5	5	5	5	5	5	5	5	5	5	5
	OUTPUT CANDIDATE	5/T			T	5/T			T	5/T			T
CAMERA SWITCH 22b, IMAGE PROCESSING 24b	FIELD	3	4	1	2	3	4	1	2	3	4	1	2
	SELECTED CAMERA	5	5	5	5	5	5	5	5	5	5	5	5
	OUTPUT CANDIDATE		T	5/T			T	5/T			T	5/T	
FINAL OUTPUT		5	T	5	T	5	T	5	T	5	T	5	T
VBI	RECORDING	1	0	1	0	1	0	1	0	1	0	1	0
	PRE-ALARM	0	*	0	*	0	*	0	*	0	*	0	*
	POST-ALARM	1	1	1	1	1	1	1	1	1	1	1	1
	ID	5	*	5	*	5	*	5	*	5	*	5	*

1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
5/T			T	5/T			T	5/T			T	5/T			T
3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2
5	5	8	8	8	8	8	8	8	8	8	8	8	8	8	8
	T	5/T			T	8/T			T	8/T			T	8/T	
5	T	5	T	5	T	8	T	5	T	8	T	5	T	8	T
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	*	0	*	0	*	0	*	0	*	0	*	0	*	0	*
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	*	5	*	5	*	8	*	5	*	8	*	5	*	8	*

T: TEST PATTERN IMAGE

The diagram illustrates a video recording and reproduction system, labeled 16. It features a central horizontal bus connecting several components. On the left, an 'IMAGE TO BE RECORDED' input feeds into a 'VIDEO ENCODER' (32), which connects to a 'DIGITAL I/F' (34). The 'DIGITAL I/F' (34) contains a 'RAM' (36) and connects to the bus. On the right, a 'REPRODUCED IMAGE' output is generated by a 'VIDEO DECODER' (38), which connects to the bus. Above the bus, a 'SUB-CPU' (40) and a 'MAIN CPU' (42) are connected via bidirectional arrows. The 'MAIN CPU' (42) includes a 'ROM' (42a). To the right of the 'MAIN CPU' is a 'JPEG CODEC' (46). Below the bus, a 'DRIVE I/F' (48) connects to an 'HDD' (50), which contains a disk (52). A 'MEMORY I/F' (54) connects to 'SDRAM' (56). On the far right, an 'OPERATION PANEL' (44) is shown, containing buttons for 'POWER' (44a), 'REC' (44b), 'PLAY_F' (44d), 'PLAY_STOP' (44f), 'REC_STOP' (44c), 'PLAY_R' (44e), and 'MENU' (44g). The 'SUB-CPU' (40) is connected to the 'OPERATION PANEL' (44) via a bidirectional arrow.

FIG. 13

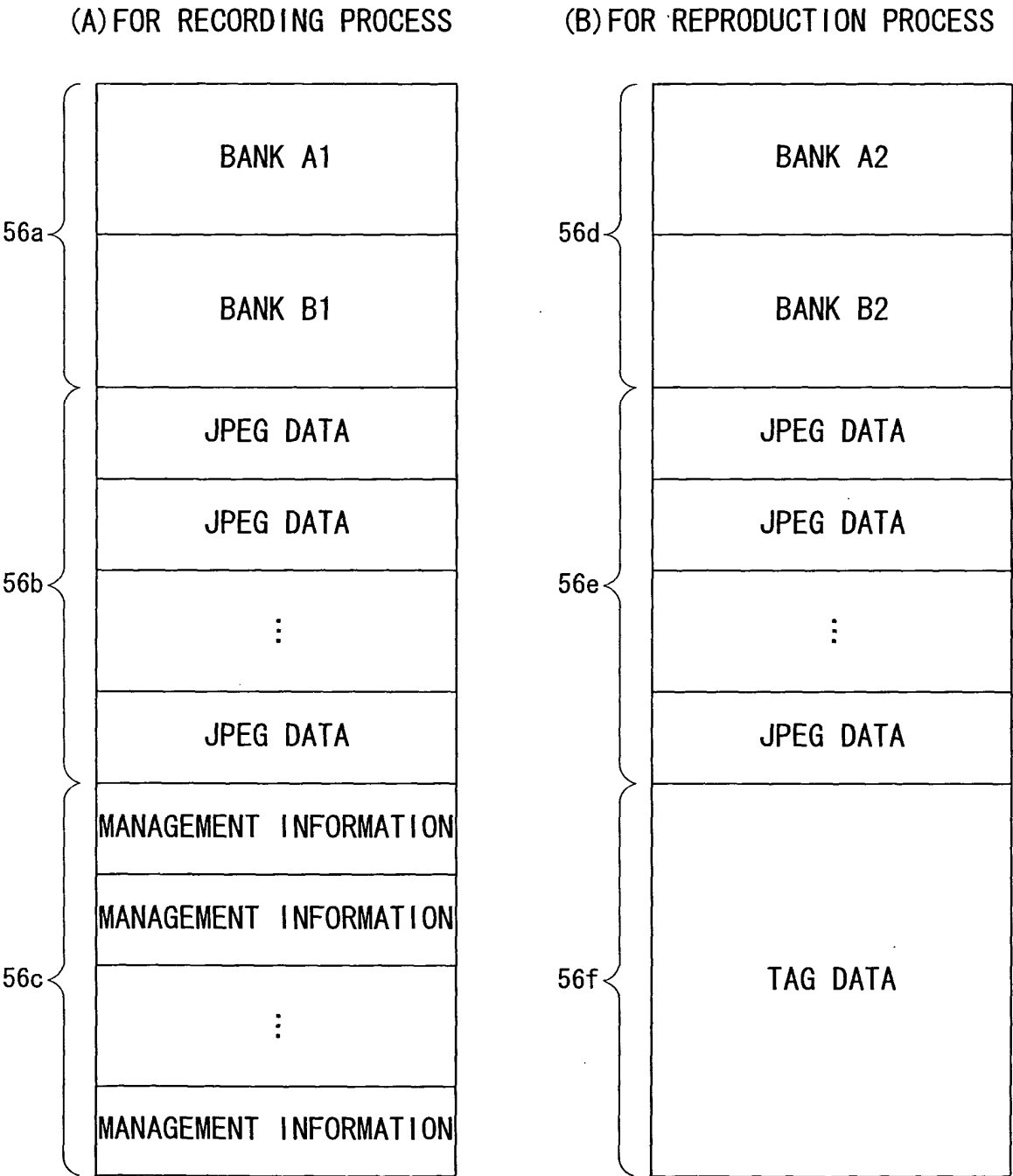


FIG. 14

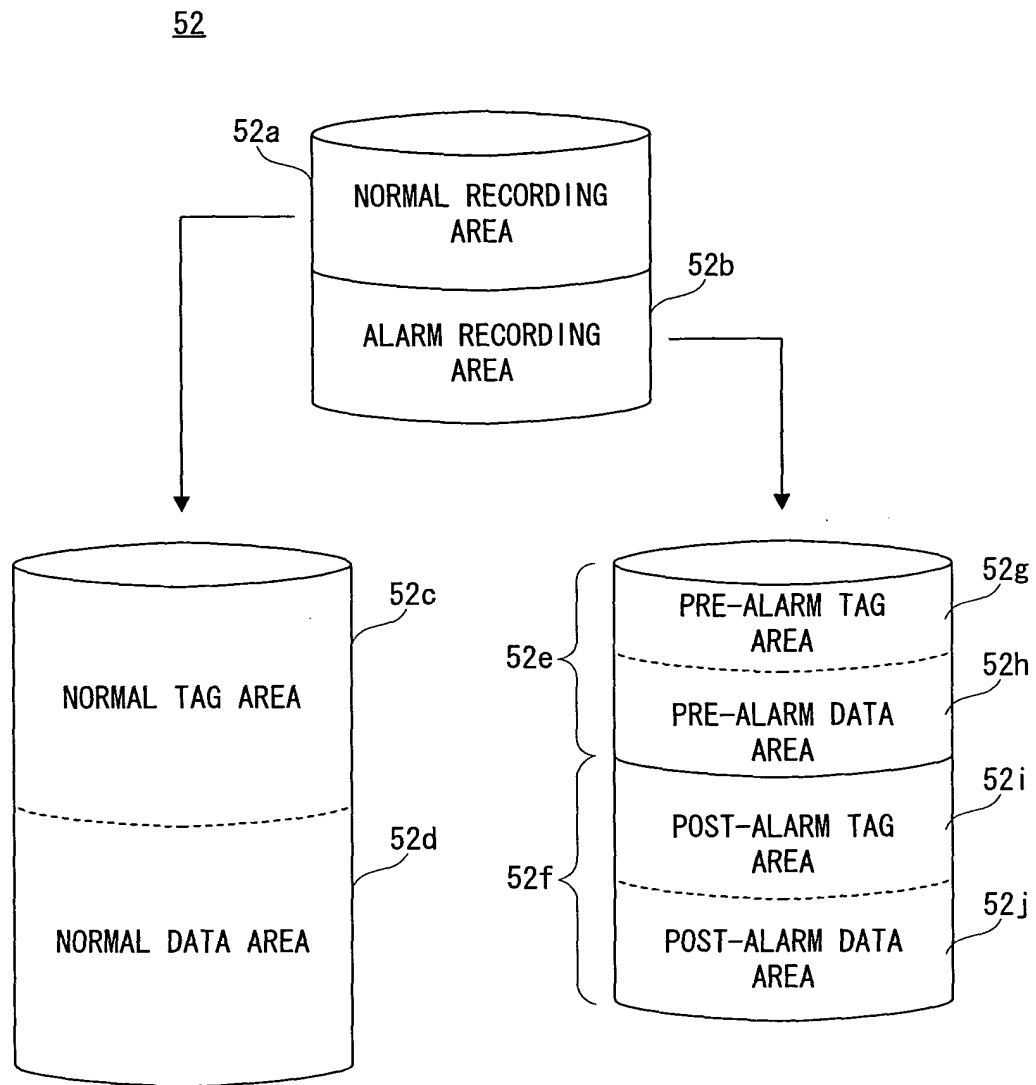


FIG. 15

(A) FIELD DATA

<p>MANAGEMENT INFORMATION (DATE, JPEG SIZE, ALARM NUMBER, CAMERA ID, RECORDING FIELD NUMBER, WAITING TIME PERIOD, etc)</p>
<p>JPEG DATA</p>

(B) TAG DATA

<p>⋮</p>
<p>MANAGEMENT INFORMATION ADDRESS (PREVIOUS FIELD)</p>
<p>JPEG DATA ADDRESS (PREVIOUS FIELD)</p>
<p>MANAGEMENT INFORMATION ADDRESS (CURRENT FIELD)</p>
<p>JPEG DATA ADDRESS (CURRENT FIELD)</p>
<p>MANAGEMENT INFORMATION ADDRESS (NEXT FIELD)</p>
<p>JPEG DATA ADDRESS (NEXT FIELD)</p>
<p>⋮</p>
<p>DATE</p>
<p>JPEG SIZE</p>
<p>ALARM NUMBER</p>
<p>CAMERA ID</p>
<p>RECORDING FIELD NUMBER</p>
<p>WAITING TIME PERIOD INFORMATION</p>
<p>⋮</p>

FIG. 16

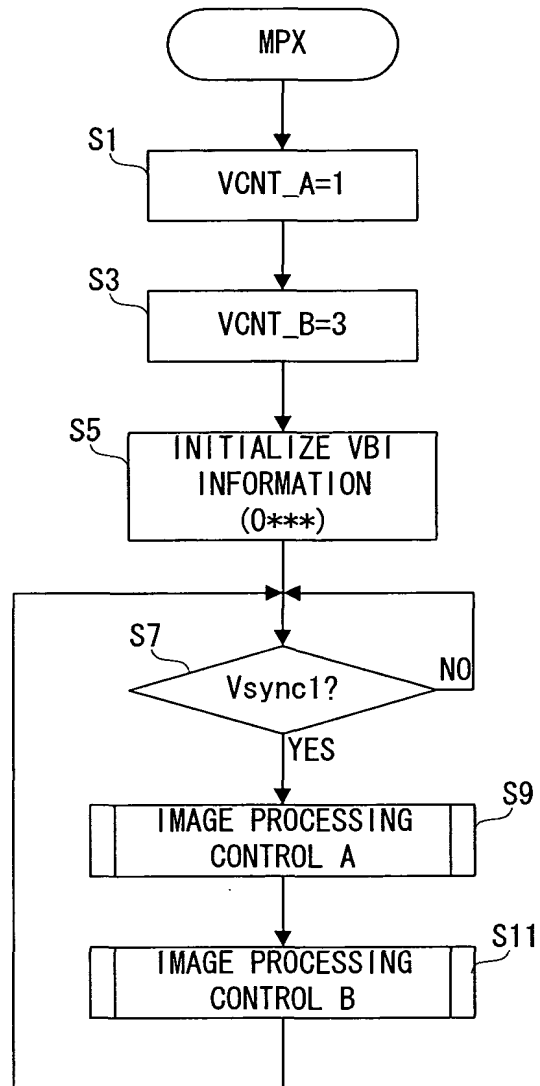


FIG. 17

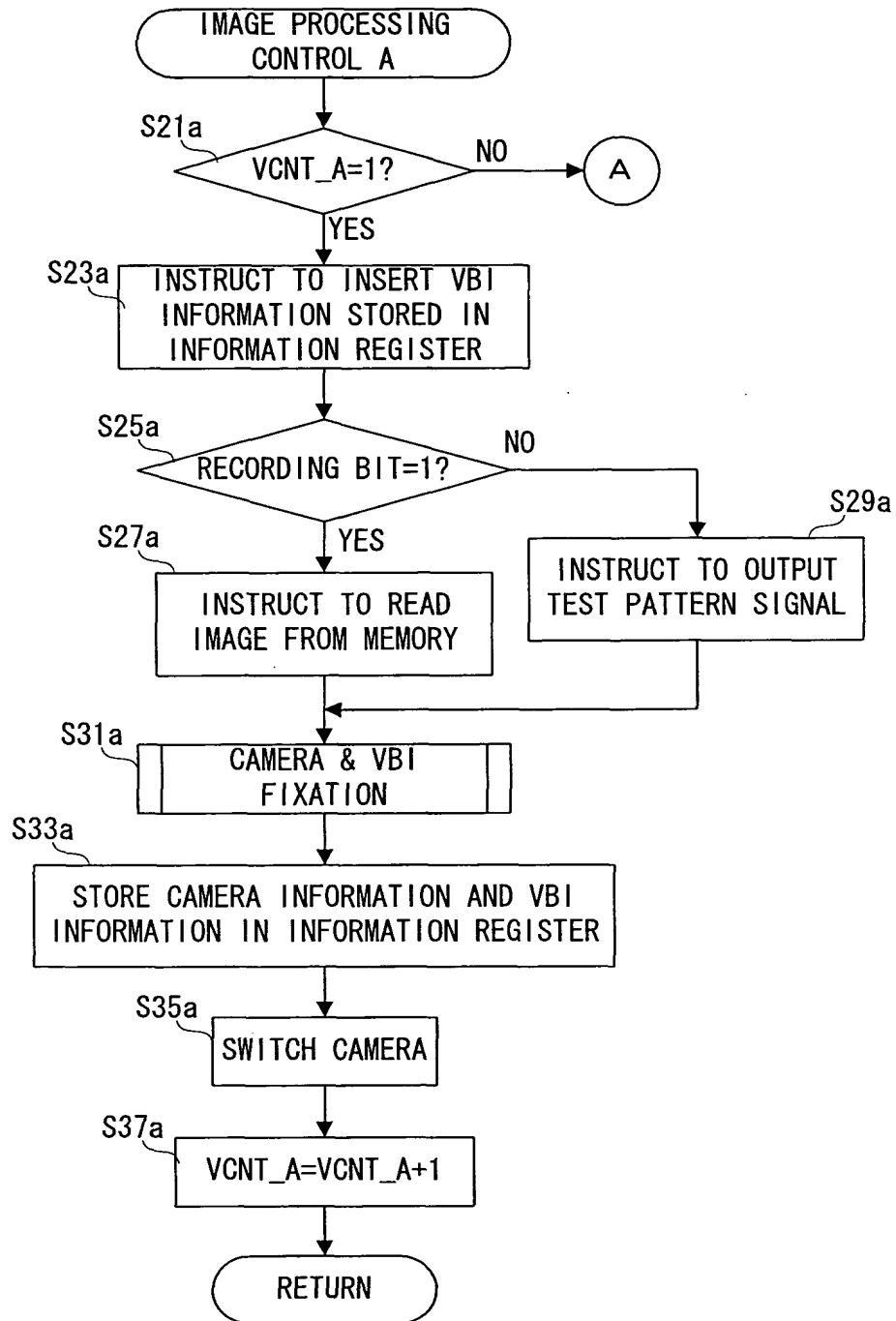


FIG. 18

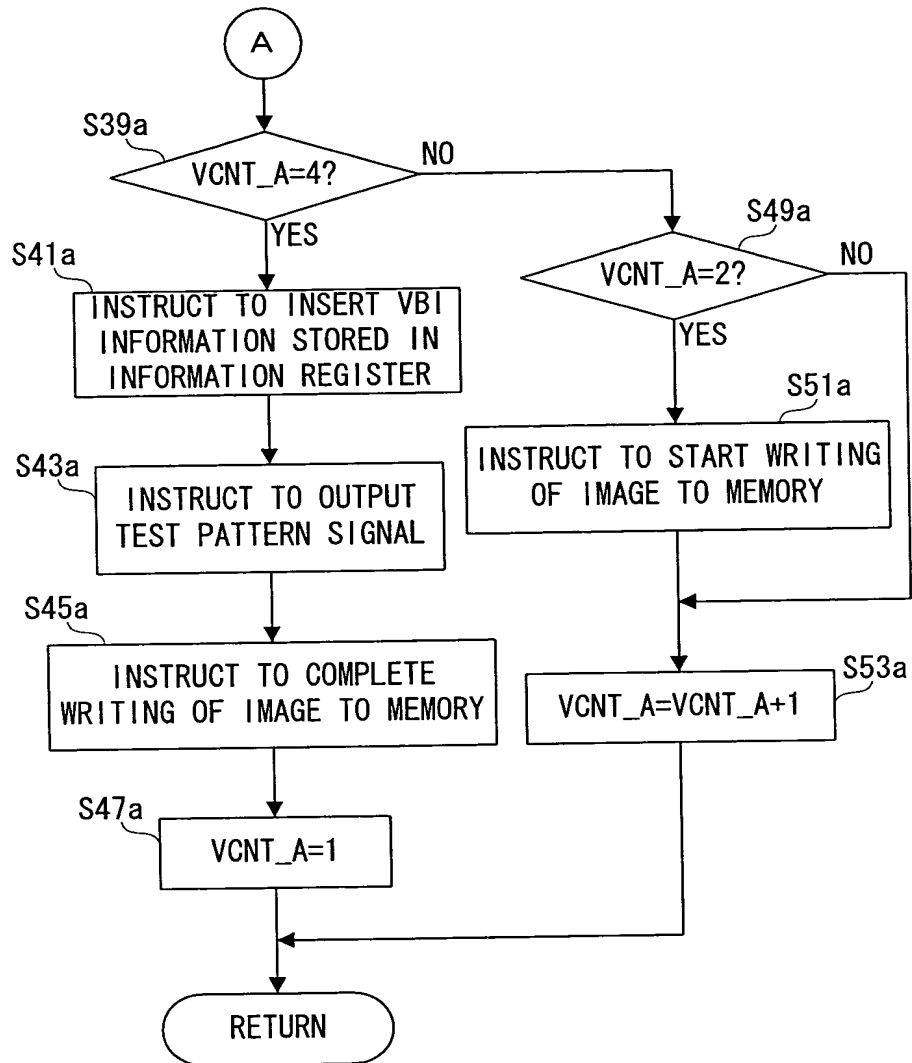


FIG. 19

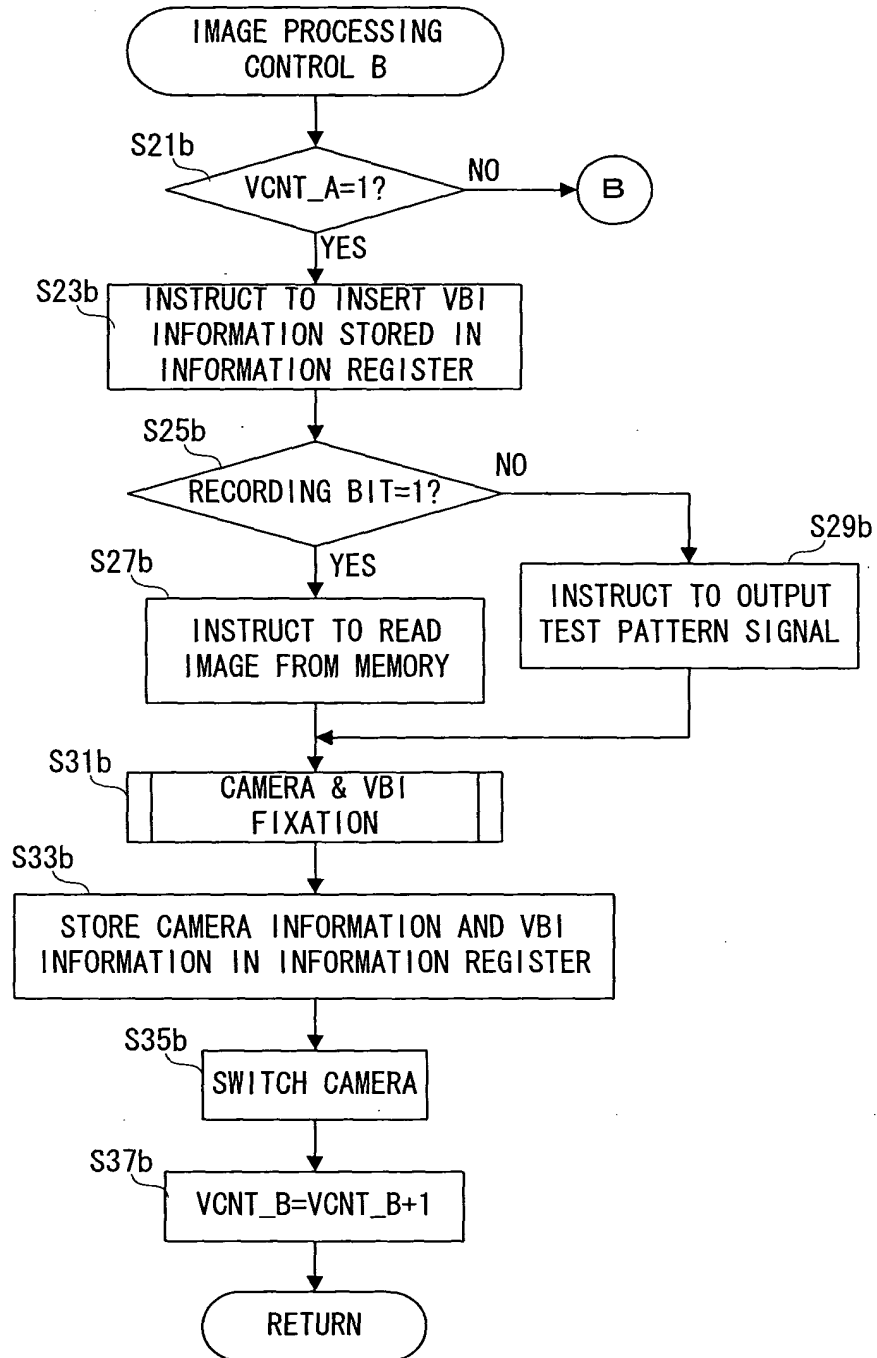


FIG. 20

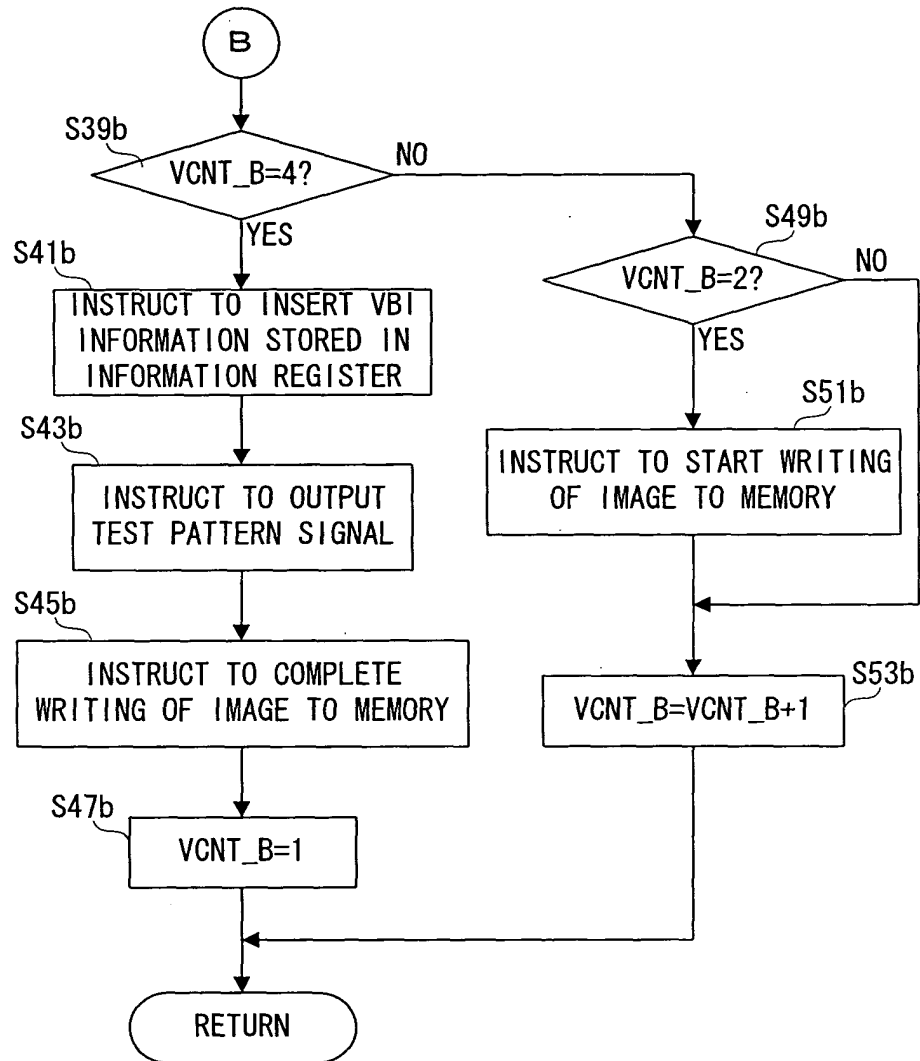


FIG. 21

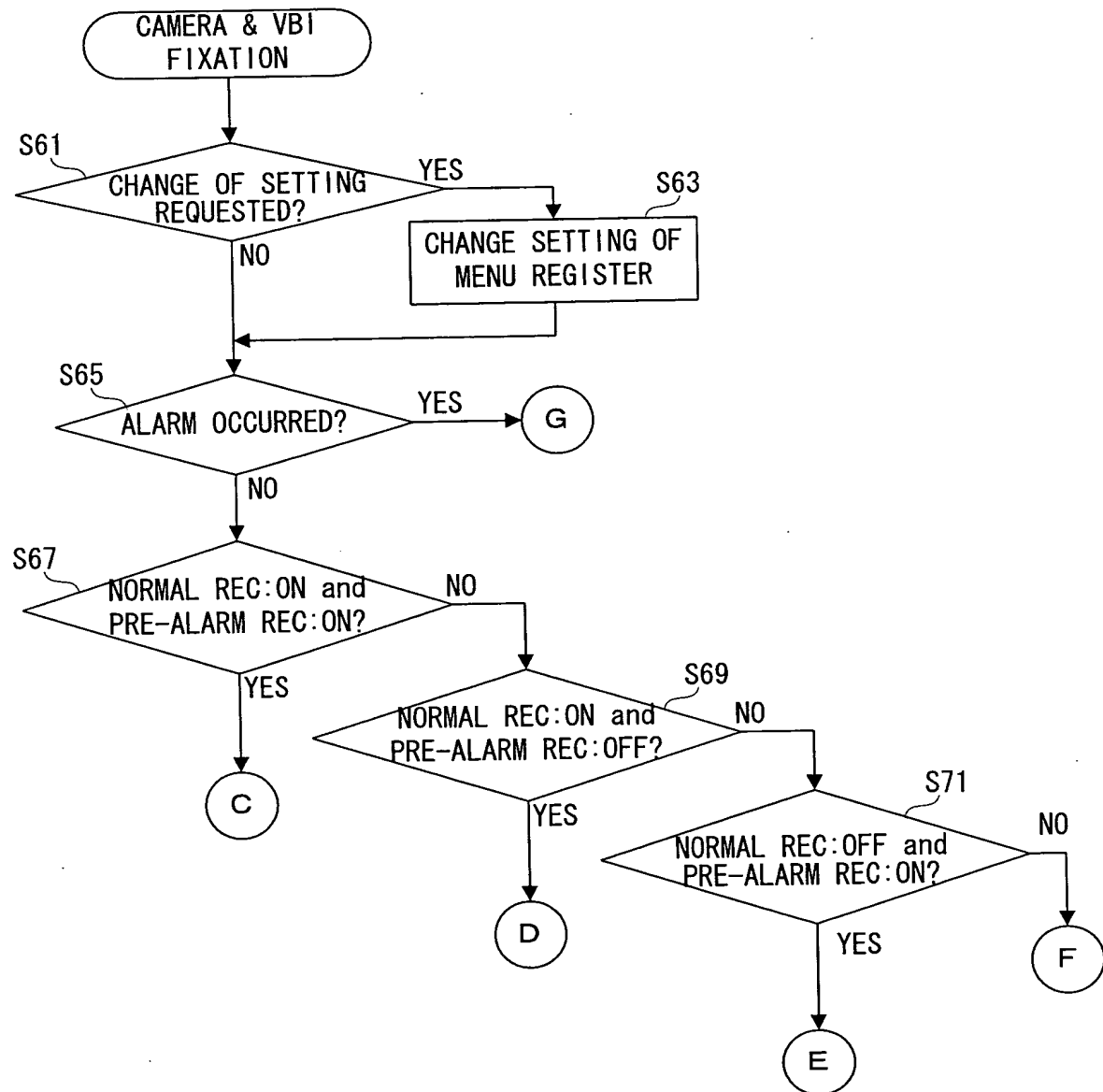


FIG. 22

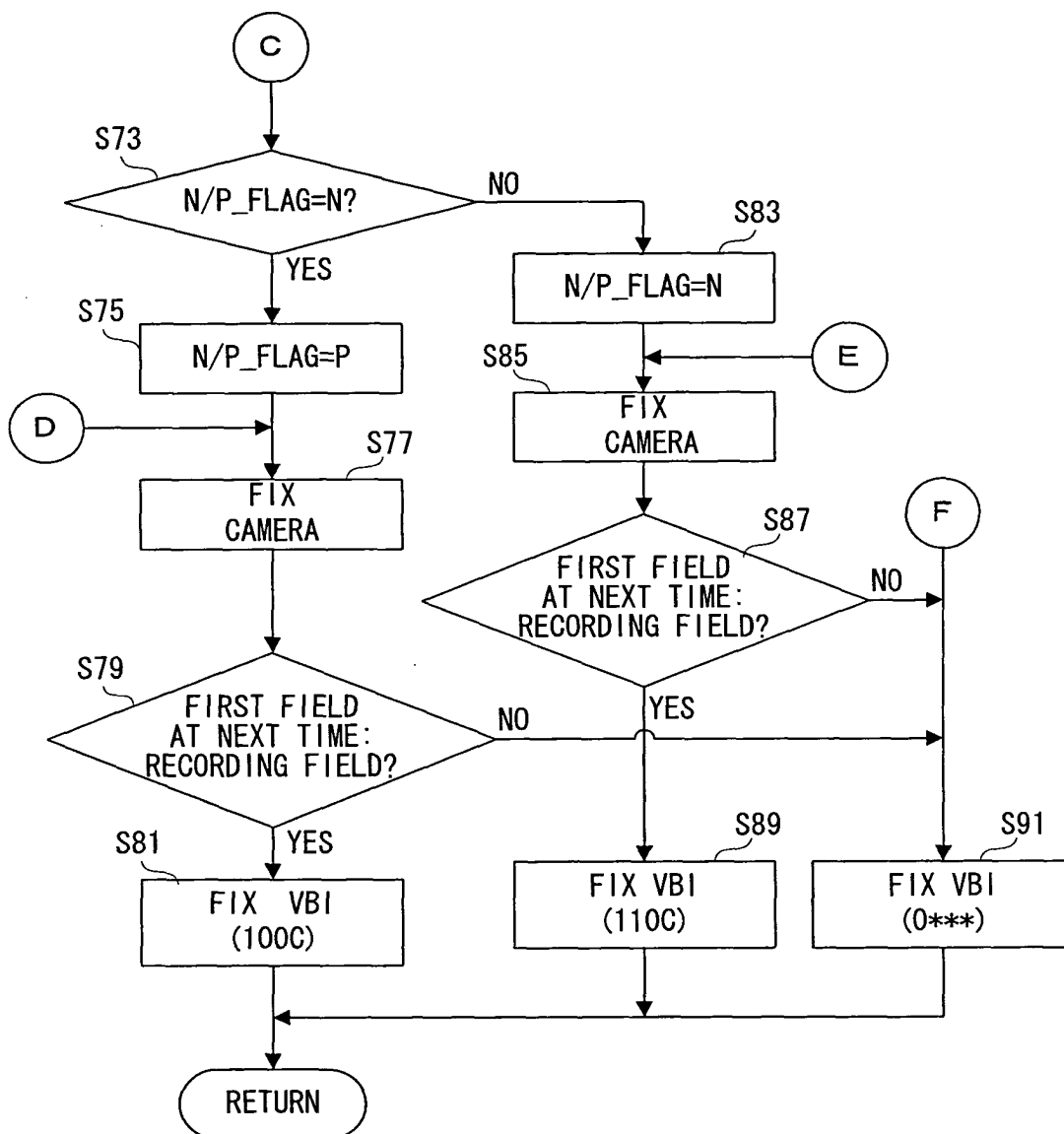


FIG. 23

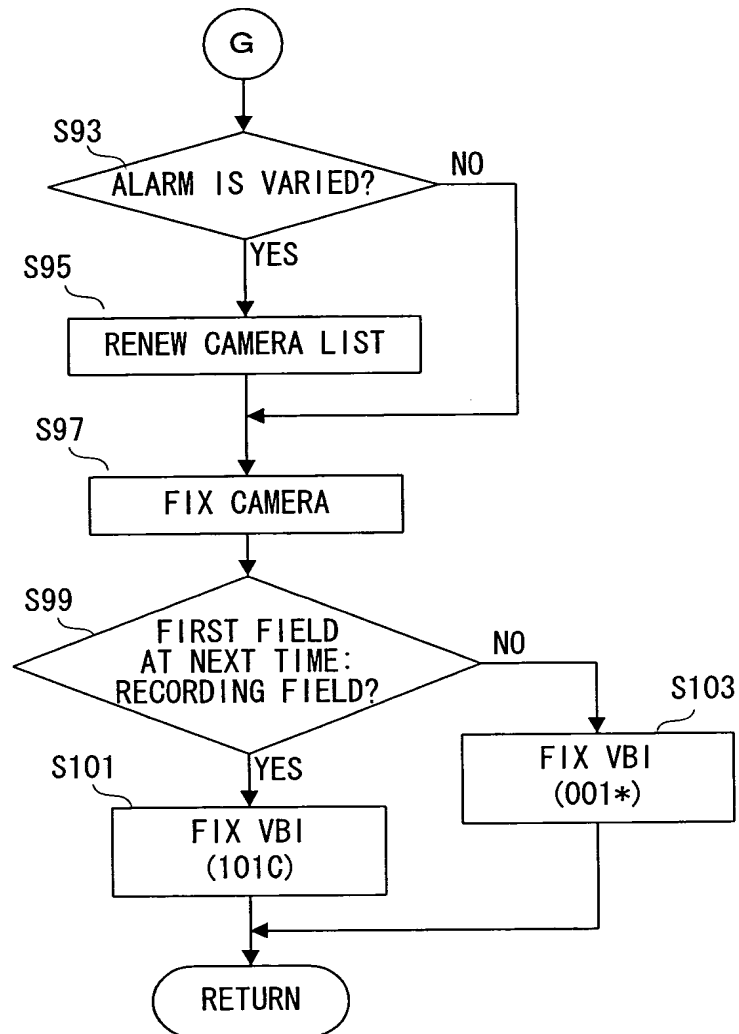


FIG. 24

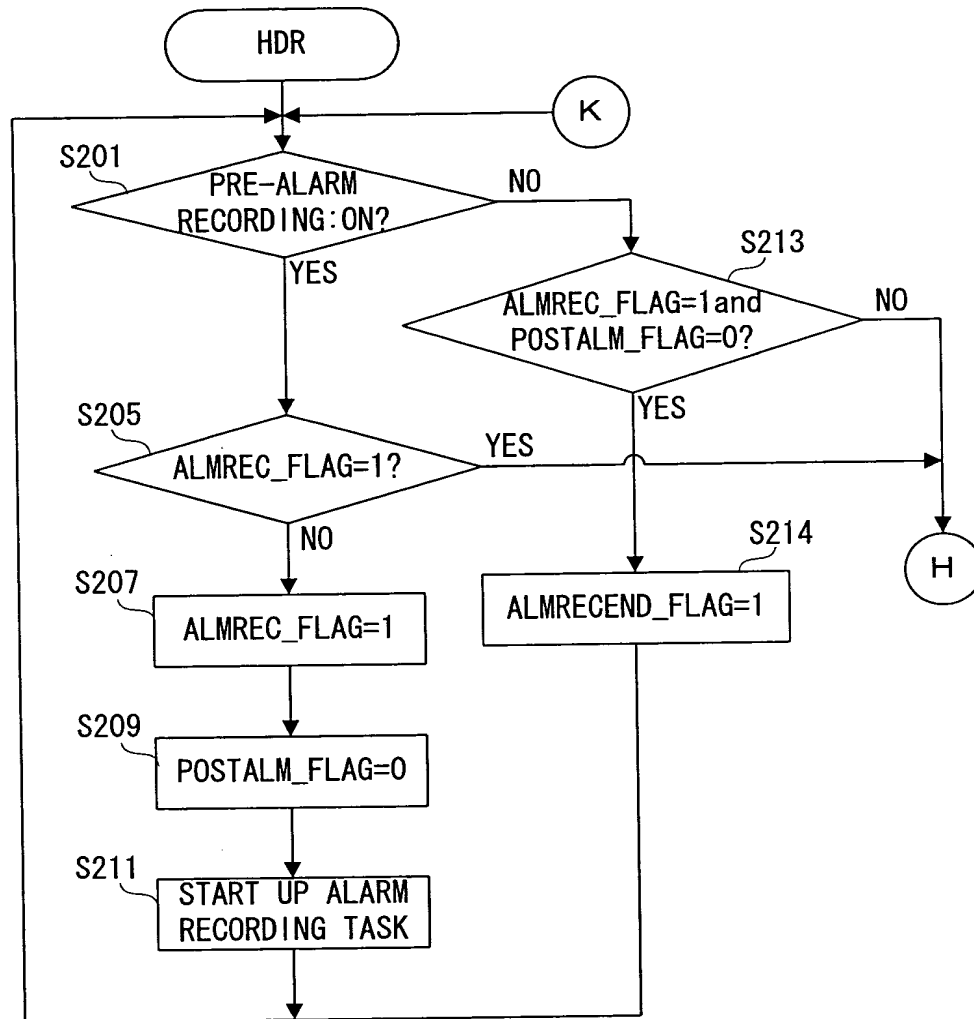


FIG. 25

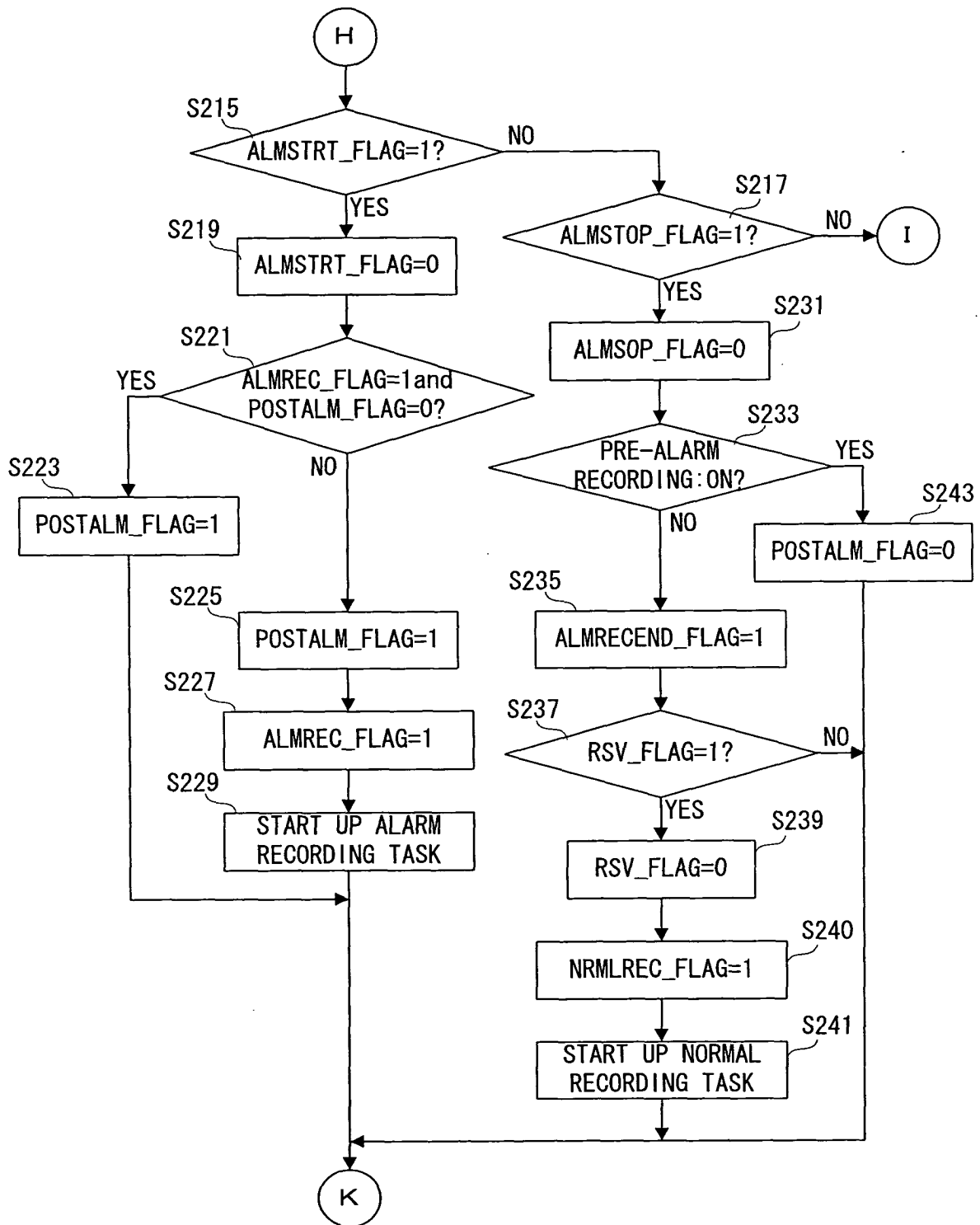


FIG. 26

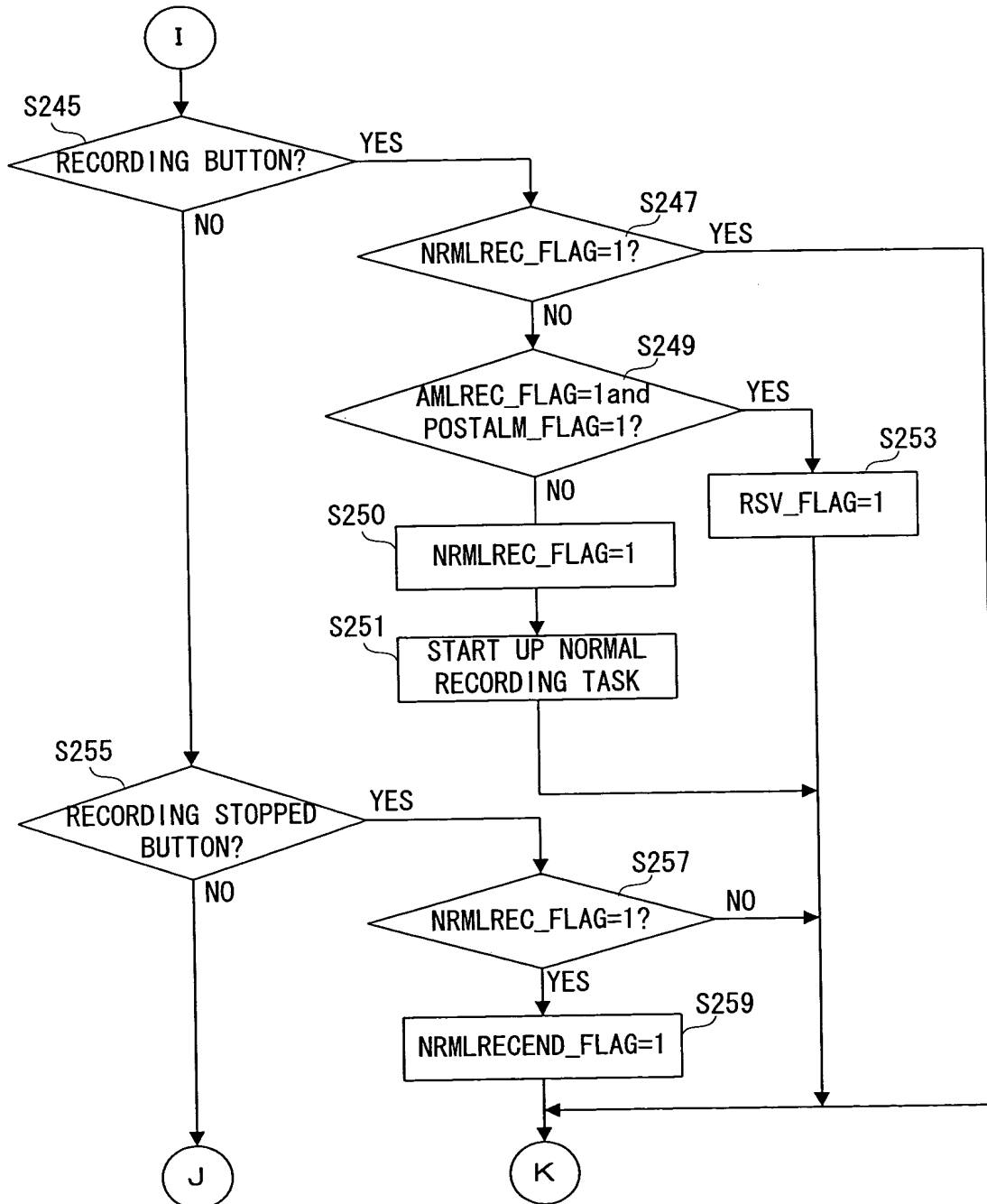


FIG. 27

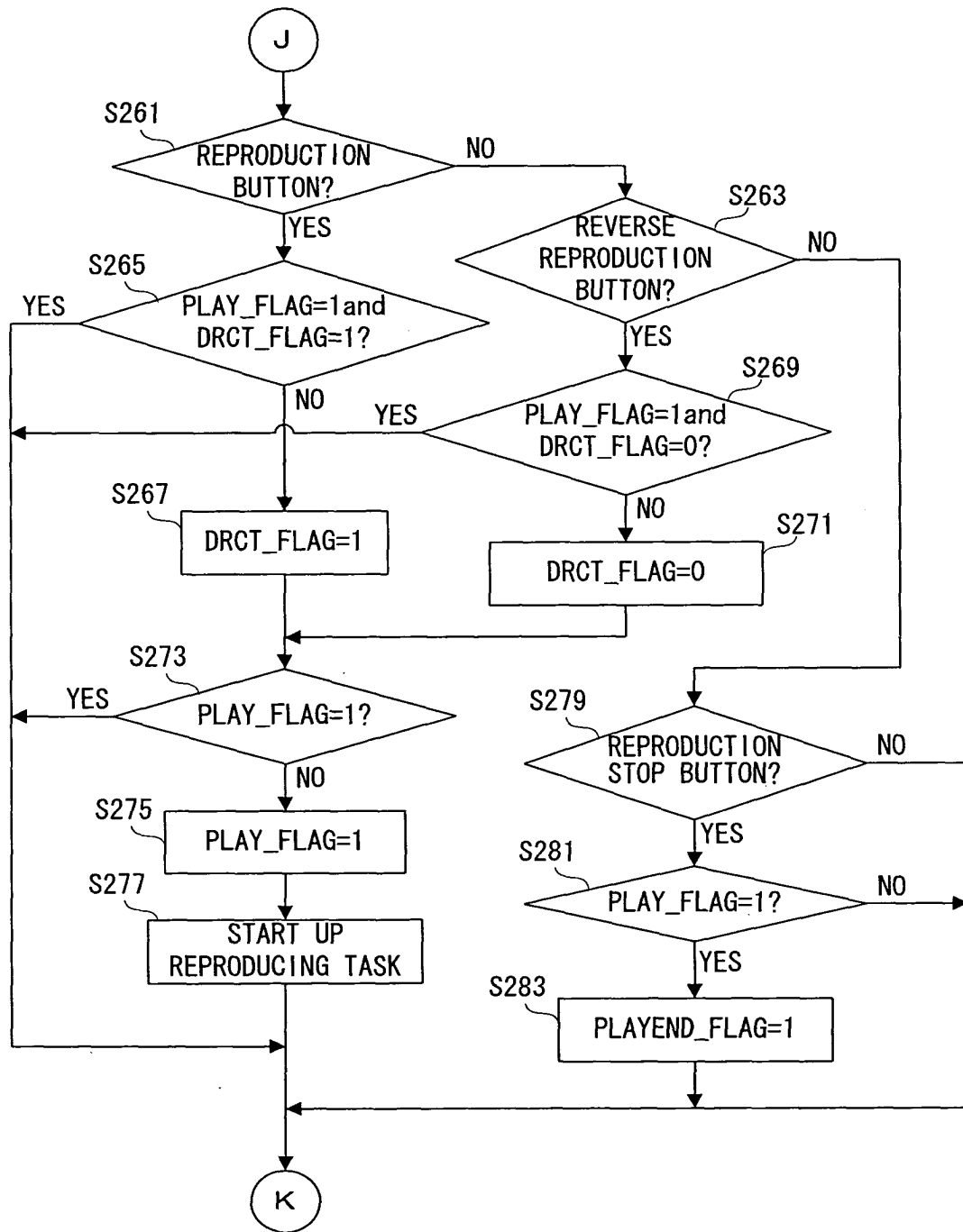


FIG. 28

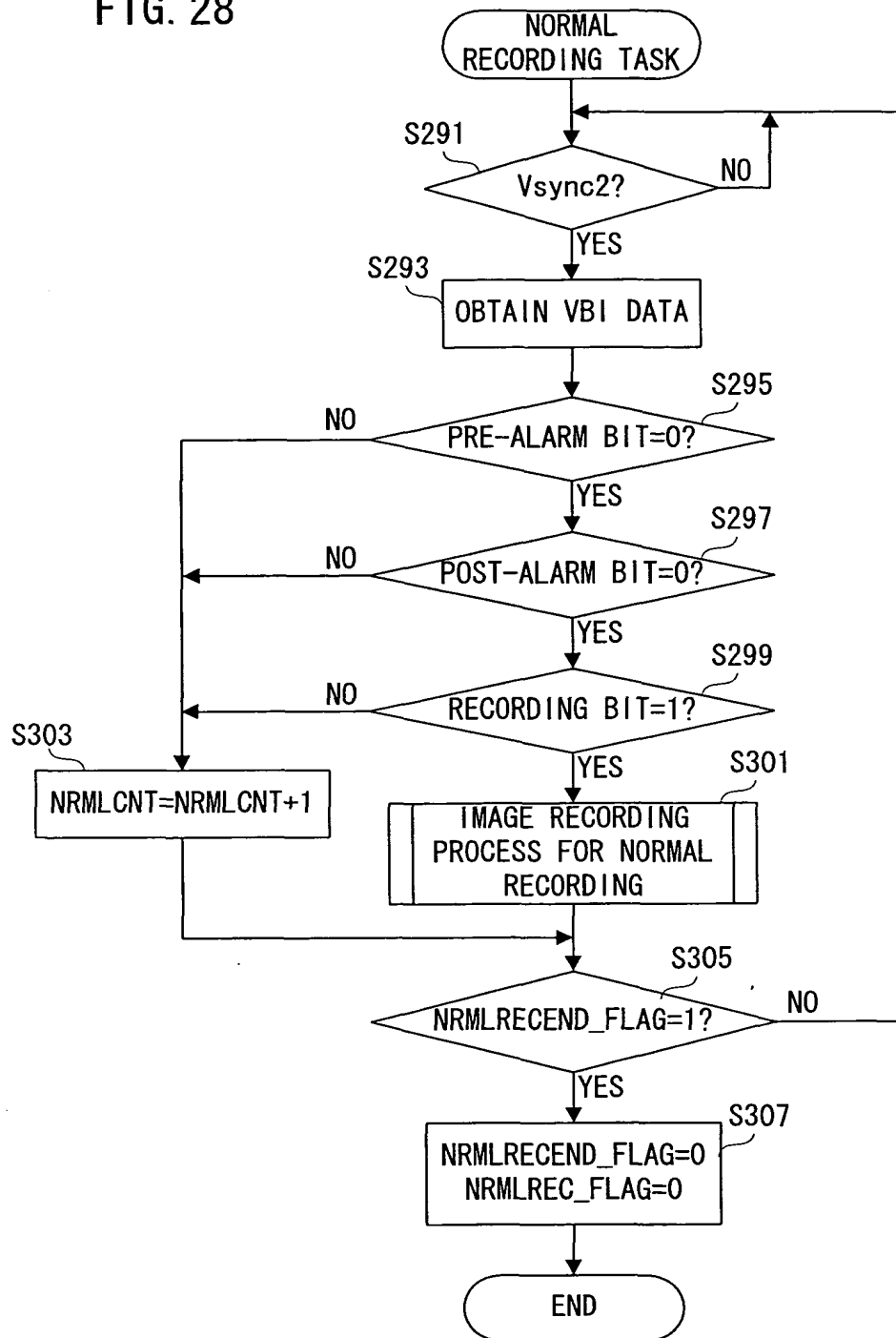


FIG. 29

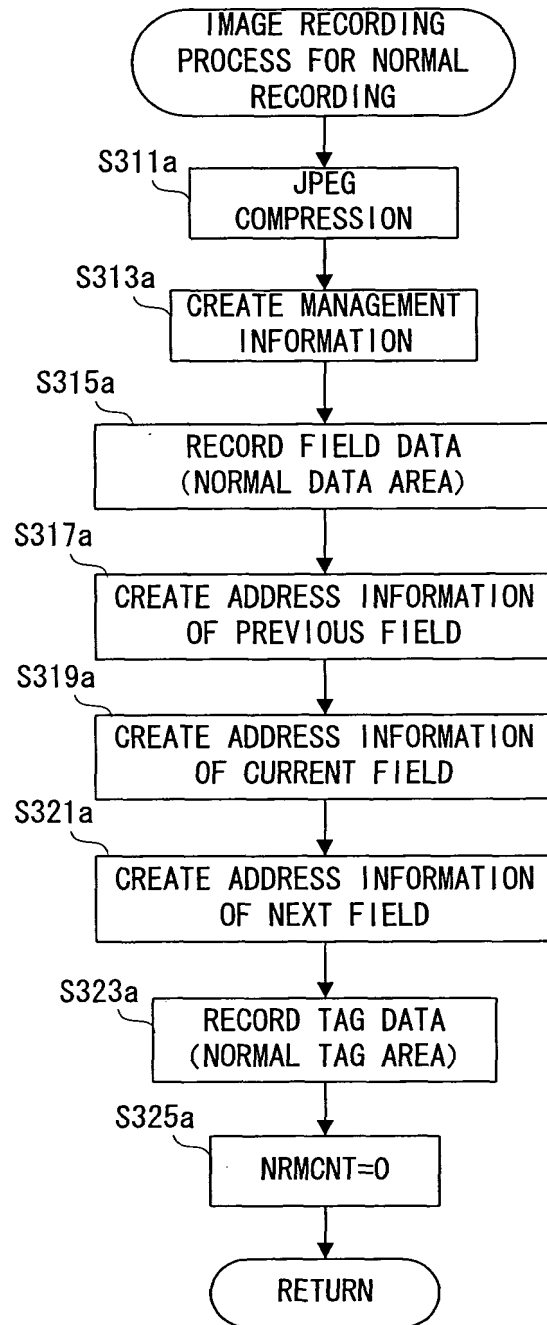


FIG. 30

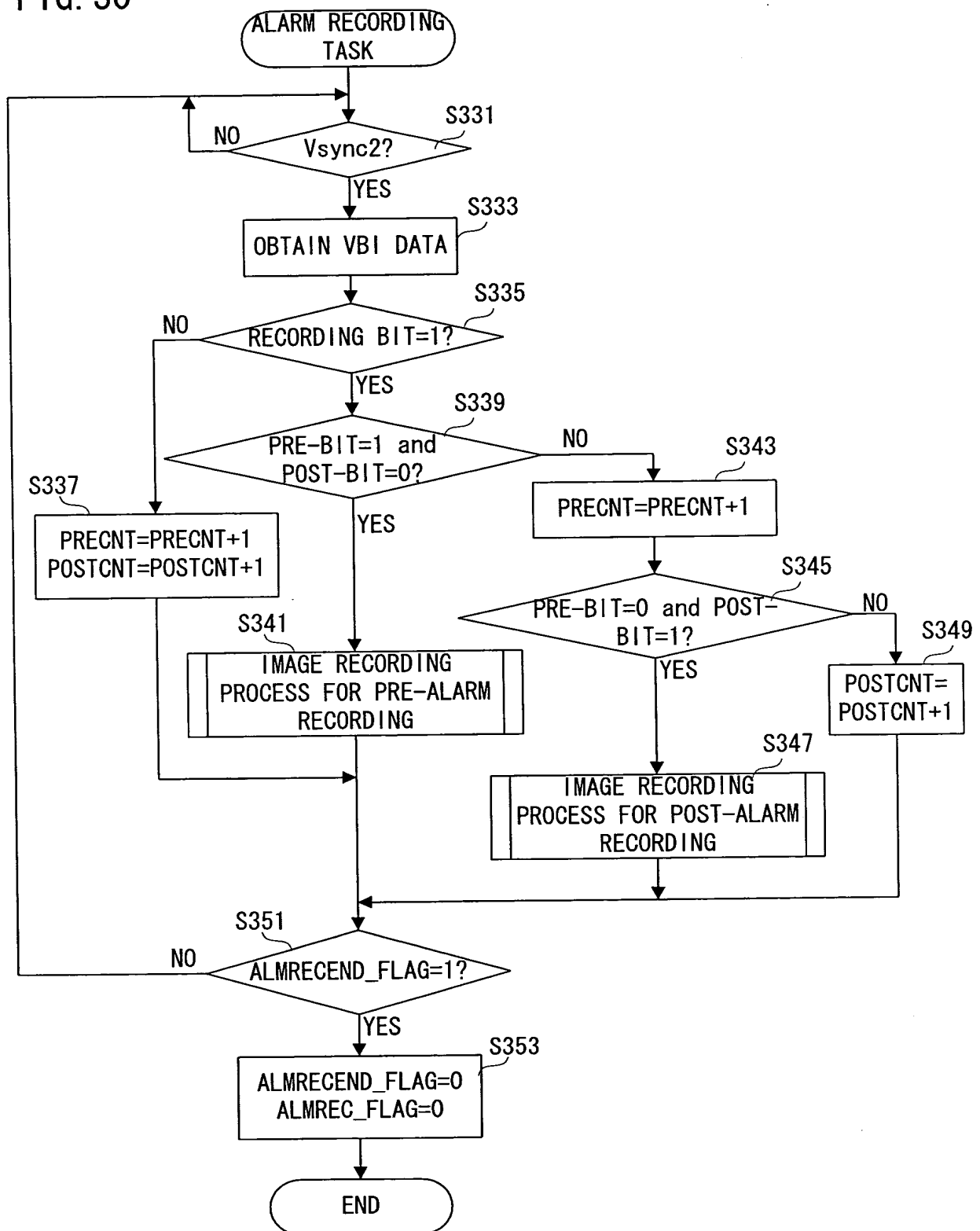


FIG. 31

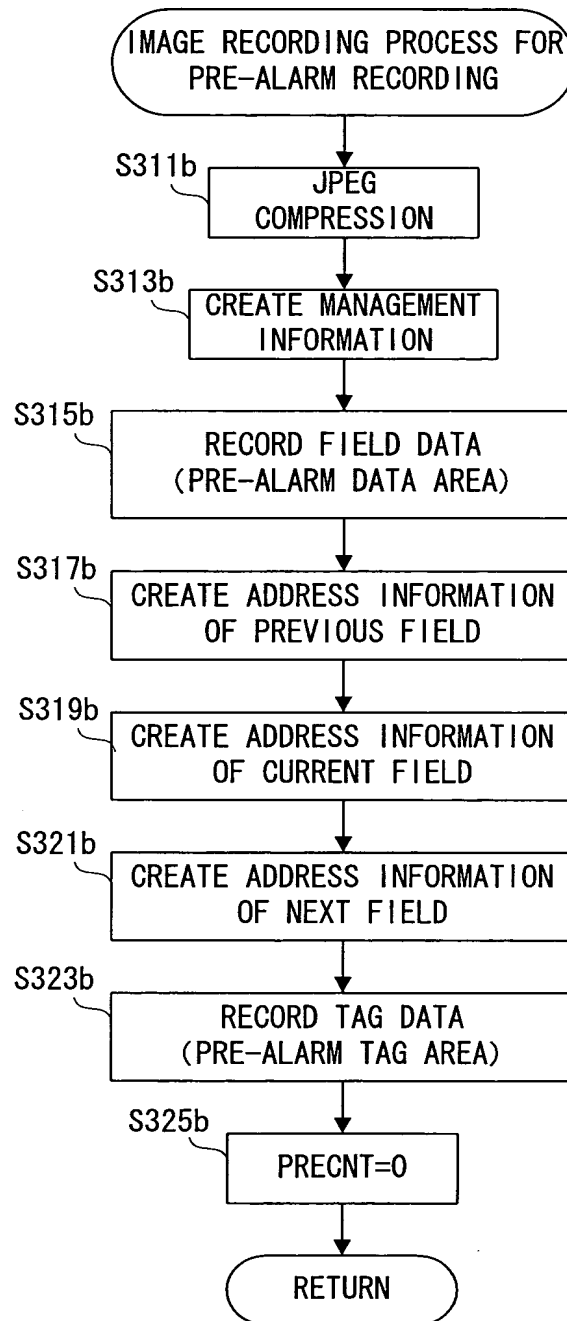


FIG. 32

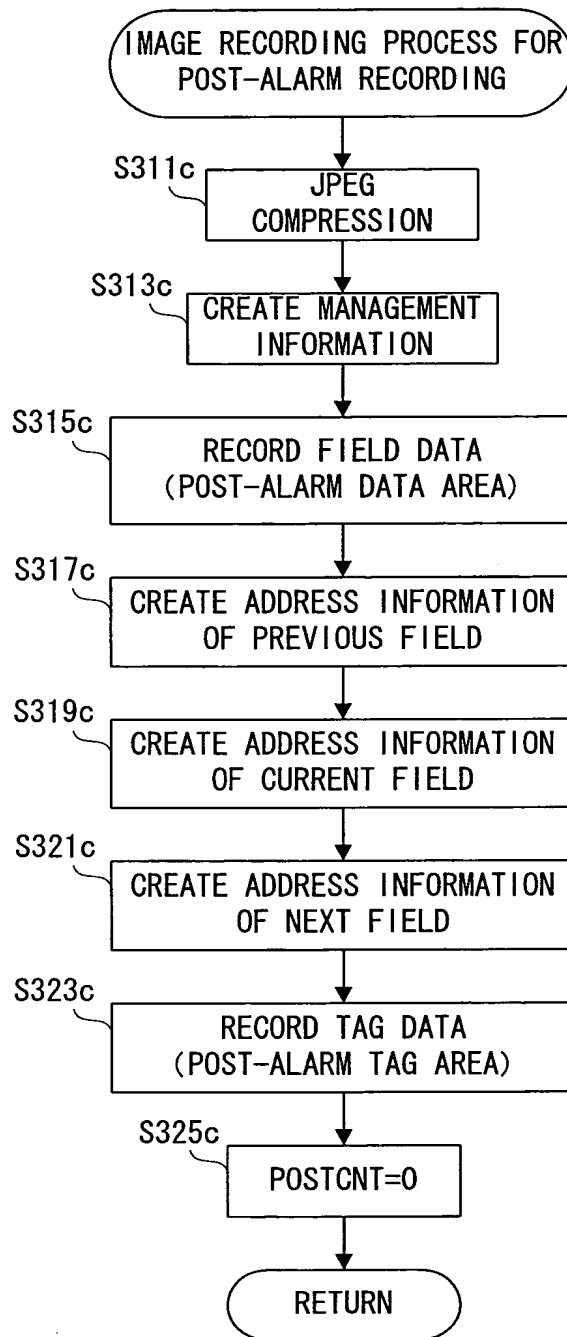


FIG. 33

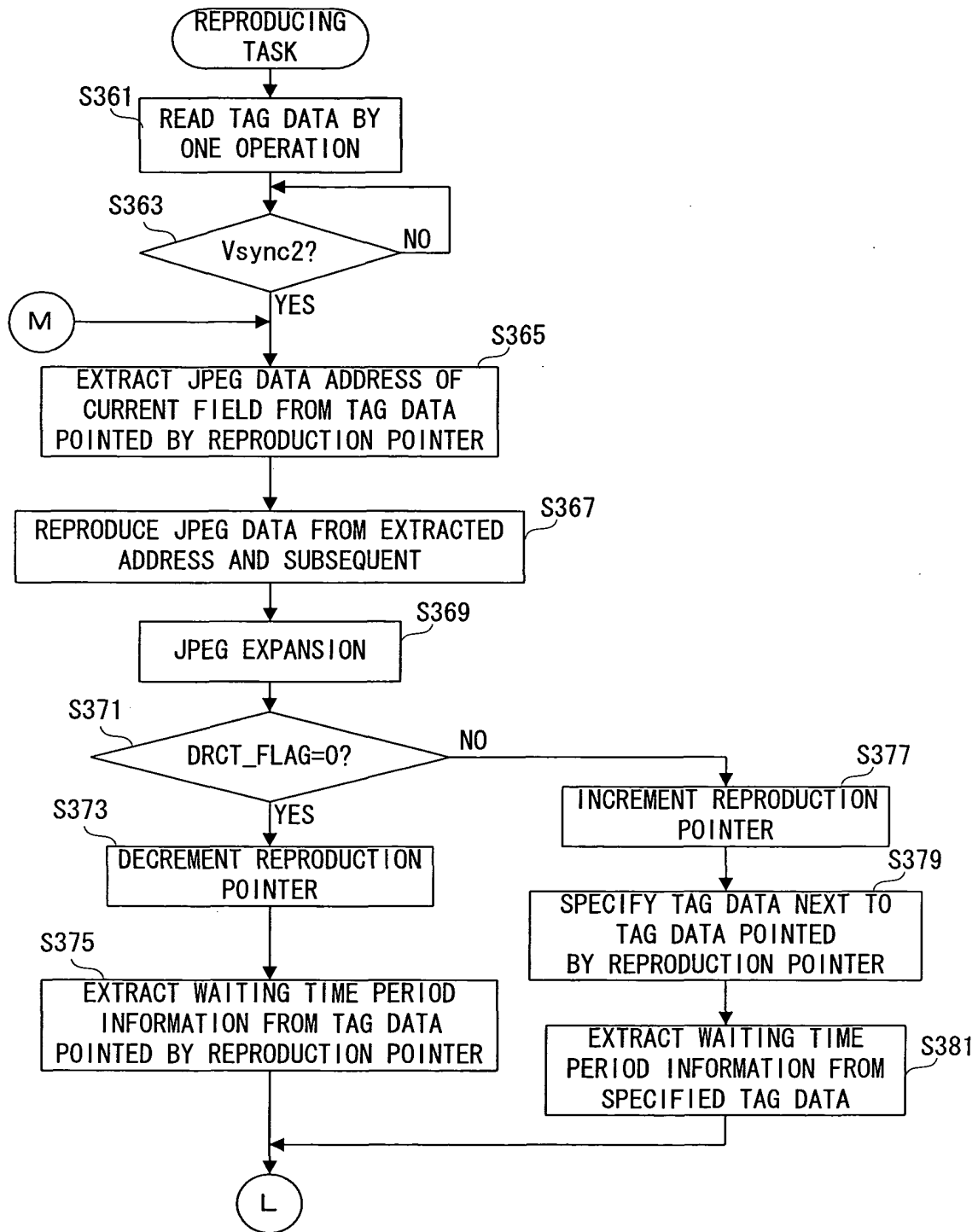


FIG. 34

